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EXAMINER	
WONG, LINDA	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/678,685	DOUMA ET AL.	
	Examiner	Art Unit	
	LINDA WONG	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *26 May 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-24 and 26-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-24,26-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Arguments

1. Applicant's arguments with respect to claims 1-26 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. **Claims 9-13,14-18,27** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

   a. **Claim 9** recites the limitation "a controller chip having a phase locked loop that is adapted to operate in a hunting mode in which the phase locked look briefly asserts a synchronization signal when a hunting frequency passes through a data signal frequency corresponding to a rate of data encoded in a data signal ..." It is unclear and indefinite as to whether the hunting frequency or data signal frequency corresponds to a rate of data encoded in a data signal.

   For the purpose of the claim rejection, the examiner will interpret the limitation as the data frequency signal corresponds to the rate at which the data signal is encoded.

   b. **Claim 14** recites the limitation "sampling data from the data signal". There are two instances of the phrase "data signal": 1) "... phase locked loop locking onto

a data signal ..." or 2) "asserting a lock signal if the phase locked loop has locked onto a data signal". Which one is being referenced?

c. **Claims 10-13,15-18,27** are rejected due to the rejection of the independent claim.

3. **Claims 14-18** are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted steps are: steps connecting sampling, extracting a clock and using the extracted clock with phase locked loop synchronization, determination steps.

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. **Claims 19-24,26-28** is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

a. **Claim 26** recites the limitation "the capacitor is coupled to the transistor such that current flows through the transistor to charge the capacitor when the synchronization signal is asserted at a rate faster than a rate at which the capacitor discharges through a resistor coupled thereto" Paragraph 30

describes the capacitor discharges at a rate slower than the rate at which it charges. Claim 20 recites the opposite.

Furthermore, claim 26 recites the limitation the capacitor charges when the synchronization signal is asserted. Paragraph 35 discloses "when it is hunting, the capacitor 44 can discharge only a small amount before the transistor 42 turns back on and charges the capacitor (i.e. resets the timer)." The paragraph indicates the capacitor would be charging as the PLL is hunting even though it is discharging a small amount until the transistor is turned back on.

b. **Claim 19** recite "a capacitor arranged to discharge when the synchronization signal is asserted ..." This is opposite of the recited limitation in claim 26. Which limitation is correct?

c. Regarding **claims 20-24,27-28**, such claims are rejected on the same basis as the rejection of the independent claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. **Claims 9-12,19-20,24-26,28** are rejected under 35 U.S.C. 102(b) as being anticipated by Lutz (U.S. Patent No.: 4276548).

a. **Claim 9**, Lutz discloses

- "an output adapted to couple to a host device" (Fig. 1, labels 22,24,12 as the host device.)
- "a controller chip having a phase locked loop that is adapted to operate in a hunting mode" (Fig. 1, label 10 shows the controller chip, label 14 as the phase locked loop, Col. 3, lines 49-65 discloses the hunting period occurs when the output on line 44 is random or noisy nature and the lock detector and timer senses the random nature of the synchronization signal, label 44 as shown in Fig. 1.)
- Hunting mode "in which the phase locked loop briefly asserts a synchronization signal when a hunting frequency passes through a data signal frequency". (Col. 3, lines 49-55 discloses hunting occurs when the synchronization of the frequency of the internal oscillator is not synchronized with the frequency of a coherent component of the difference signal.)
- wherein the data signal frequency "corresponding to a rate of data encoded in a data signal" (Col. 3, lines 4-50 discloses the phase locked loop synchronizes the frequency of the internal oscillator with the amplified difference signal or data signal received from the speaker shown in Fig. 1, label 12. Since the phase locked loop is synchronizing the data signal with the internal clock, the data signal frequency would correspond to the data rate encoded in the data signal received by the speaker in Fig. 1, label 12.)

- "and that is adapted to operate in a locked mode in which the phase locked loop asserts the synchronization signal so long as the phase locked loop is locked onto a data signal" (Col. 3, lines 49-65 discloses the phase locked loop outputs a constant level DC signal when the is synchronized. "Lock detector and timer includes suitable circuitry for sensing the random nature of the lock signal and for developing on the line a stabilization signal of predetermined period after the lock signal has stabilized.")
- "a translation circuit adapted to convert the synchronization signal from the controller chip to a lock signal usable by the host device" (Fig. 1, labels 16,18,20 converts the synchronization signal from the controller chip, label 14 to a lock signal usable by the host device, labels 22,24,12.)
- "wherein a logic level of the lock signal is asserted when the phase locked loop is locked onto a data signal and is de-asserted when the phase locked loop asserts the synchronization signal in hunting mode." (Fig. 1, label 16 shows a lock detector and timer. Col. 3, lines 49-65 disclose "Lock detector and timer includes suitable circuitry for sensing the random nature of the lock signal and for developing on the line a stabilization signal of predetermined period after the lock signal has stabilized." Lines 49-55 disclose the hunting mode occurrence.)

b. **Claim 10**, Lutz discloses "the translation circuit comprising a timer adapted to measure a period of time that the synchronization signal is asserted." (Fig. 1, label 16 and 18 for resetting the timing.)

c. **Claims 11,12**,

- Lutz discloses "an input level detector that compares the synchronization signal with a reference signal and produces logical signals within the timing circuit". (Fig. 3a, label 16, timing circuit, shows an operational amplifier or comparator, label 300, for receiving the synchronization signal, label 44, and comparing the signal with a reference signal, input to label +. Col. 8, lines 8-15 discloses "lacking the random excursions, the signal will no longer cause the potential developed at the inverting input of the operational-amplifier 300 to exceed the potential developed at its non-inverting input.")

d. **Claim 19**, Lutz discloses

- "a timing circuit adapted to measure a period of time that the synchronization signal is asserted using at least a capacitor, wherein the timing circuit is further adapted to generate an output signal having a voltage across the capacitor" (Col. 3, lines 55-60 discloses "Lock detector and timer 16 includes suitable circuitry for sensing the random nature of the lock signal and for developing on a line 46 a (stabilization signal) of predetermined period after the lock signal has stabilized." Col. 8, lines 8-15 discloses "lacking the random excursions, the signal will no longer cause the potential developed at the inverting input of the operational-amplifier 300 to exceed the potential developed at its non-inverting input." Col. 8, lines 19-22 discloses "A predetermined time after synchronization is

achieved, the potential developed across capacitor 318 will rise to a level which will trigger timer 18 ..." Fig. 3a, label 318 shows the Voltage of the output would be across the such a capacitor. Fig. 3b, label 18 shows the timer, which sends information to label 16, Fig. 3a, through label E.)

- "a comparator circuit adapted to compare the output signal with a reference signal such that a lock signal is not asserted unless the comparison of the output signal with the reference signal indicates that the period of time that the synchronization signal is asserted exceeds a minimum period of time" (Col. 3, lines 55-60 discloses "Lock detector and timer 16 includes suitable circuitry for sensing the random nature of the lock signal and for developing on a line 46 a (stabilization signal) of predetermined period after the lock signal has stabilized." Col. 8, lines 8-15 discloses "lacking the random excursions, the signal will no longer cause the potential developed at the inverting input of the operational-amplifier 300 to exceed the potential developed at its non-inverting input.")
- Wherein the capacitor is "arranged to discharge when the synchronization signal is asserted and to charge when the synchronization signal is not asserted" (Col. 8, lines 55-67 discloses when the PLL synchronizes the internal clock with the data signal, the capacitor discharges. Since the capacitor discharges when the PLL is synchronized, the capacitor would charge when the PLL is hunting.)

e. **Claim 20**, Lutz discloses "the timing circuit comprises a transistor that is controlled by the synchronization signal for resetting the timing circuit such that the capacitor discharges." (Fig. 1, label 18 is a timer for resetting the timing circuit, label 16, wherein the timer has a transistor, Fig. 3b, label 342. Fig. 3a, label 16 shows the synchronization signal controls the lock detector and timing component, label 16. Based on the information from the synchronization signal, label 16 outputs information to label 18, timer, where the transistor determines resetting mode.)

f. **Claim 24**, Lutz discloses "an input level detector that passes the synchronization signal to the timing circuit when the synchronization signal exceeds a reference voltage." (Col. 3, lines 55-60 discloses "Lock detector and timer 16 includes suitable circuitry for sensing the random nature of the lock signal and for developing on a line 46 a (stabilization signal) of predetermined period after the lock signal has stabilized." Col. 8, lines 8-15 discloses "lacking the random excursions, the signal will no longer cause the potential developed at the inverting input of the operational-amplifier 300 to exceed the potential developed at its non-inverting input." Col. 8, lines 19-22 discloses "A predetermined time after synchronization is achieved, the potential developed across capacitor 318 will rise to a level which will trigger timer 18 ..." Fig. 3a, label 318 shows the Voltage of the output would be across the such a capacitor.)

g. **Claim 28**, Lutz discloses "the capacitor is arranged such that a voltage across the capacitor is an average of the synchronization signal over a period of time". (Col. 9, lines 12-25, discloses when line 352 is low, the capacitor is charging for a predetermined time. Col. 8, lines 8-22, discloses the timer 18 is triggered after a period of time where synchronization has been achieved. Col. 8, lines 55-64 discloses the synchronization state of the PLL causes a low potential on line 352, and as discussed above, line 352 determines the charging of the capacitor. When the state is changed, line 352 is changed. Thus, the predetermined amount of time the capacitor is charging depends on the amount of time synchronization is achieved. Thus, the voltage across the capacitor would be an average of the synchronization signal over a period of time.)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claims 1-3,6-7** are rejected under 35 U.S.C. 103(a) as being unpatentable over Lutz (US Patent No.: 4276548) in view of Khoury, Jr. et al (US Publication No.: 20040042504).

a. **Claim 1**, Lutz discloses:

- "a controller chip that includes a phase locked loop adapted to operate in a hunting mode and a locked mode" (Fig. 1, label 10 shows the controller chip, label 14 as the phase locked loop, Col. 3, lines 49-65 discloses the hunting period occurs when the output on line 44 is random or noisy nature and the lock detector and timer senses the random nature of the synchronization signal, label 44 as shown in Fig. 1.)
- "wherein, the phase locked loop is further adapted to assert a synchronization signal in the hunting mode when a hunting frequency passes through a data signal frequency" (Col. 3, lines 49-55 discloses hunting occurs when the synchronization of the frequency of the internal oscillator is not synchronized with the frequency of a coherent component of the difference signal.)
- "wherein the phase locked loop is further adapted to keep the synchronization signal asserted as long as the phase locked loop is locked onto a data signal" (Col. 3, lines 49-65 discloses the phase locked loop outputs a constant level DC signal when the is synchronized. "Lock detector and timer includes suitable circuitry for sensing the random nature of the lock signal and for developing on the line a stabilization signal of predetermined period after the lock signal has stabilized.")
- "a timing circuit adapted to measure a period of time that the synchronization signal is asserted and to produce a lock signal if the synchronization signal is asserted for at least a specified period of time"

(Fig. 1, label 16 shows a lock detector and timer. Col. 3, lines 49-65 disclose "Lock detector and timer includes suitable circuitry for sensing the random nature of the lock signal and for developing on the line a stabilization signal of predetermined period after the lock signal has stabilized.")

- Lutz fails to disclose "a demultiplexer arranged to receive a clock signal from the phase locked loop, the demultiplexer being configured to convert the serial data signal to a parallel data signal based on the clock signal."
- Khoury, Jr. et al discloses such a limitation. (Fig. 2, label 48a as the demux and label ck1 as the clock from the phase locked loop, wherein label 48a outputs parallel signals Dout1 and Dout2.)

b. **Claim 2**, Lutz discloses "the timing circuit is an analog timer comprising a capacitor and resistor network." (Fig. 3a, label 16 shows the lock detector and timer, wherein the block has a network of resistors and capacitors.)

c. **Claim 3**, Lutz discloses "the timing circuit comprises a transistor for resetting the timing circuit" (Fig. 1, label 18 is a timer for resetting the timing circuit, label 16, wherein the timer has a transistor, label 342.)

d. **Claim 6**

- Lutz discloses "an input level detector that compares the synchronization signal with a reference signal and produces logical signals within the timing circuit". (Fig. 3a, label 16, timing circuit, shows an operational amplifier or comparator, label 300, for receiving the synchronization signal, label 44,

and comparing the signal with a reference signal, input to label +. Col. 8, lines 8-15 discloses "lacking the random excursions, the signal will no longer cause the potential developed at the inverting input of the operational-amplifier 300 to exceed the potential developed at its non-inverting input.")

e. **Claim 7**,

- Lutz discloses "a comparator that receives a signal from the capacitor and resistor network and a reference signal as input and that outputs the lock signal to the host device based on the value of the reference signal compared to the signal from the capacitor and resistor network". (Fig. 3a, label 16, timing circuit, shows an operational amplifier or comparator, label 300, for receiving the synchronization signal, label 44, and comparing the signal with a reference signal, input to label +. Col. 8, lines 8-15 discloses "lacking the random excursions, the signal will no longer cause the potential developed at the inverting input of the operational-amplifier 300 to exceed the potential developed at its non-inverting input." Fig. 3a, label 16 shows a network of capacitors and resistors connected to the comparator or operational amplifier, label 300.)

7. **Claims 14-16,27** are rejected under 35 U.S.C. 103(a) as being unpatentable over Lutz (US Patent No.:) in view of the admitted prior art (pages 2-5).

a. **Claim 14**, Lutz discloses

- receiving an asserted synchronization signal from a phase locked loop, the phase locked loop disposed on the controller chip (Fig. 1, label 10 shows the controller chip, label 44 as the synchronization signal outputted from label 14, phase locked loop.);
- determining whether the synchronization signal is caused by the phase locked loop locking onto a data signal or by the phase locked loop passing a hunting frequency through a data signal frequency (Col. 3, lines 49-65 discloses the hunting period occurs when the output on line 44 is random or noisy nature and the lock detector and timer senses the random nature of the synchronization signal, label 44 as shown in Fig. 1.)
- asserting a lock signal if the phase locked loop has locked onto a data signal (Col. 3, lines 55-60 discloses the lock detector and timer determines whether the synchronization signal is stabilized after a predetermined period.)
- Lutz fails to disclose
    1. "sampling data from the data signal"
    2. "extracting a clock signal from the data signal;" and
    3. "using the extracted clock signal as a reference for converting the sampled signal into synchronized data to be read by the host device"
- The admitted prior art discloses a microcontroller for sampling the data, extracting a clock signal from the data, using the clock as a reference for synchronizing the data, wherein the synchronization is performed using a

PLL as described in paragraphs 6 and 7. It would have been obvious to one skilled in the art at the time of the invention sample and extract a clock of the data signal for the purpose of synchronization as disclosed by the prior art into Lutz so to accurately read the data at appropriate times allowing for efficient synchronization.

b. **Claim 15**, Lutz discloses

- "measuring a period of time that the synchronization signal is asserted" (Col. 8, lines 8-15 discloses "lacking the random excursions, the signal will no longer cause the potential developed at the inverting input of the operational-amplifier 300 to exceed the potential developed at its non-inverting input.")
- "determining that the synchronization signal is caused by the phase locked loop locking onto the data signal if the period of time that the synchronization signal is asserted is greater than a specified period of time." (Col. 3, lines 55-60 discloses "Lock detector and timer 16 includes suitable circuitry for sensing the random nature of the lock signal and for developing on a line 46 a (stabilization signal) of predetermined period after the lock signal has stabilized.")

c. **Claim 16**, Lutz discloses "comparing the asserted synchronization signal with a reference signal to determine if the asserted synchronization signal is produced by the phase locked loop locking onto a data signal or by the phase locked loop passing a hunting frequency through the data signal frequency." (Col. 3, lines

55-60 discloses "Lock detector and timer 16 includes suitable circuitry for sensing the random nature of the lock signal and for developing on a line 46 a (stabilization signal) of predetermined period after the lock signal has stabilized." Col. 3, lines 49-55 describes the hunting mode.)

d. **Claim 27**, Lutz fails to disclose "wherein the data signal is an electronic data signal, the fiber-optic transponder further comprising circuitry to convert optical data signal to the electronic data signal".

- The admitted prior art discloses such a limitation. (Paragraph 3) It would have been obvious to one skilled in the art to combine the components found in Lutz as discussed in claim 9 and components of a fiber optical transponder as disclosed by the admitted prior art so provide information to a computer using fiber optic cables so to provide efficient synchronization within a computer system.

8. **Claims 4,5** are rejected under 35 U.S.C. 103(a) as being unpatentable over Lutz in view of Khoury, Jr et al as applied to claims 1,14, respectively, in view of Transistors Non-Patent Literature.

a. **Claim 4**, Lutz fails to disclose the type of transistors used in his timer, however, Transistors Non-Patent Literature discloses transistor is at least one of a PNP and NPN bipolar junction transistor (p. 3, The NPN Transistor). Because NPN transistor are well known in the art as low cost transistor with low power consumption at low voltage levels, it would have been obvious to one skilled in

the art at the time of invention to incorporate a NPN transistor as disclosed by Transistors Non-Patent Literature into the combined invention disclosed by Lutz.

b. **Claim 5**, Lutz fails to disclose the type of transistors used in his timer, however, Transistors Non-Patent Literature discloses transistor is a field effect transistor (p. 3, FET's as Transistors). Because FET transistor are well known in the art as low cost transistor which can operate at high voltage levels, it would have been obvious to one skilled in the art at the time of invention to incorporate a FET transistor as disclosed by Transistors Non-Patent Literature into the combined invention disclosed by Lutz.

9. **Claim 21** is rejected under 35 U.S.C. 103(a) as being unpatentable over Lutz as applied to claim 19, in view of Transistors Non-Patent Literature.

a. **Claim 21**, Lutz fails to disclose the type of transistors used in his timer, however, Transistors Non-Patent Literature discloses transistor is at least one of a PNP and NPN bipolar junction transistor (p. 3, The NPN Transistor). Because NPN transistor are well known in the art as low cost transistor with low power consumption at low voltage levels. It would have been obvious to one skilled in the art at the time of invention to incorporate a NPN transistor as disclosed by Transistors Non-Patent Literature into the combined invention disclosed by Lutz.

10. **Claim 26** is rejected under 35 U.S.C. 103(a) as being unpatentable over Lutz as applied to claim 19.

    a. **Claim 26**, Lutz discloses

    - "the capacitor is coupled to the transistor such that current flows through the transistor to" discharge "the capacitor when the synchronization signal is asserted at a rate faster than a rate at which the capacitor" charges "through a resistor coupled thereto" (Fig. 3b, label 342 as the transistor, label 360 as the capacitor, Col. 8, lines 45-67 describes the functionality of the circuit shown in Fig. 3b, label 18. Col. 8, lines 64-67 discloses the transistor provides a path to discharge the capacitor when the PLL has synchronized the data signal to the internal clock. As described in Col. 8, lines 45-67, when the potential on label 352 is high, the transistor is saturated, causing the transistor to act as a short. A certain amount of current will pass through the shorted line as well as the capacitor. When the potential on line 352 is low, the transistor is turned off or the switch is open. The total amount of current will pass through the capacitor, thus the capacitor will charge at a higher rate than the discharge rate.)
    - "the comparator circuit is adapted to assert the lock signal when the voltage across the capacitor exceeds the reference signal" (Col. 3, lines 55-60 discloses "Lock detector and timer 16 includes suitable circuitry for sensing the random nature of the lock signal and for developing on a line 46 a (stabilization signal) of predetermined period after the lock signal has

stabilized." Col. 8, lines 8-15 discloses "lacking the random excursions, the signal will no longer cause the potential developed at the inverting input of the operational-amplifier 300 to exceed the potential developed at its non-inverting input.")

- Due to the 35 USC 112, 1st paragraph rejection of the independent claim, Lutz uses a NPN transistor wherein it would have been obvious to one skilled in the art to use a PNP transistor since the functionality of a PNP is the inverse of the NPN and can perform the same functionalities, thus allowing the circuit as soon in Fig. 3b to provide timing information, wherein the timing information would efficient locking information.

11. **Claim 17** is rejected under 35 U.S.C. 103(a) as being unpatentable over Lutz in view of the admitted prior art as applied to claim 14, in view of Rumbaugh (US Patent No. 6275144).

    a. **Claim 17**,

    - Lutz discloses "comparing the lock signal with a reference signal to produce the lock signal useful by a host device". (Fig. 3a, label 16, timing circuit, shows an operational amplifier or comparator, label 300, for receiving the synchronization signal, label 44, and comparing the signal with a reference signal, input to label +. Col. 8, lines 8-15 discloses "lacking the random excursions, the signal will no longer cause the potential developed at the inverting input of the operational-amplifier 300 to exceed the potential

developed at its non-inverting input." Fig. 1, labels 22,24,12 shows the host device.)

- Lutz fails to disclose the host device is connected to a fiber optic transponder.
- Rambaugh discloses connection using fiber optics. (Fig. 3 shows the connections. Col. 4, lines 39-41 discloses a fiber optic interface device.) It would have been obvious to one skilled in the art at the time of the invention to connect the system as shown by Lutz to a fiber optics device as shown by Rumbaugh so to provide better and quicker transmission.

12. **Claim 8** is rejected under 35 U.S.C. 103(a) as being unpatentable over Lutz in view of Khourdy, Jr et al as applied to claim 7, further in view of IBM Technical Disclosure Bulletin, May 1990.

a. **Claim 8**,

- Lutz fail to disclose a comparator includes feedback that changes a logical level of the lock signal output to the host device when the value of the lock signal changes by some value greater than a hysteresis threshold value.
- IBM Technical Disclosure Bulletin, May 1990 discloses a comparator includes feedback that changes a logical level of the lock signal output to the host device when the value of the lock signal changes by some value greater than a hysteresis threshold value (see part 3 and figure 2). The disclosure further states that this scheme has the advantage of providing a

stabilized synchronization acquisition (part 3, lines 2-3). Because of this advantage it would have been obvious to one skilled in the art a the time of invention to incorporate the phase lock as disclosed by the IBM Technical Disclosure Bulletin, May 1990 into the combined invention of Lutz and Lee.

13. **Claims 13,22,23** are rejected under 35 U.S.C. 103(a) as being unpatentable over Lutz as applied to claims 7,12,14,19,22, respectively, in view of IBM Technical Disclosure Bulletin, May 1990.

    a. **Claim 13**, Lutz fails to disclose a comparator includes feedback that changes a logical level of the lock signal output to the host device when the value of the lock signal changes by some value greater than a hysteresis threshold value. However, IBM Technical Disclosure Bulletin, May 1990 discloses a comparator includes feedback that changes a logical level of the lock signal output to the host device when the value of the lock signal changes by some value greater than a hysteresis threshold value (see part 3 and figure 2). The disclosure further states that this scheme has the advantage of providing a stabilized synchronization acquisition (part 3, lines 2-3). Because of this advantage it would have been obvious to one skilled in the art a the time of invention to incorporate the phase lock as disclosed by the IBM Technical Disclosure Bulletin, May 1990 into the combined invention of Lutz and Lee.

    b. **Claims 22, 23**, Lutz fails to disclose a comparator includes feedback that changes a logical level of the lock signal output to the host device when the

value of the lock signal changes by some value greater than a hysteresis threshold value. However, IBM Technical Disclosure Bulletin, May 1990 discloses a comparator includes feedback that changes a logical level of the lock signal output to the host device when the value of the lock signal changes by some value greater than a hysteresis threshold value (see part 3 and figure 2). The disclosure further states that this scheme has the advantage of providing a stabilized synchronization acquisition (part 3, lines 2-3). Because of this advantage it would have been obvious to one skilled in the art a the time of invention to incorporate the phase lock as disclosed by the IBM Technical Disclosure Bulletin, May 1990 into the combined invention of Lutz.

14. **Claim 18** is rejected under 35 U.S.C. 103(a) as being unpatentable over Lutz in view of the admitted prior art as applied to claim 14, respectively, in view of IBM Technical Disclosure Bulletin, May 1990.

    a. **Claim 18,** Lutz fails to disclose a comparator includes feedback that changes a logical level of the lock signal output to the host device when the value of the lock signal changes by some value greater than a hysteresis threshold value. However, IBM Technical Disclosure Bulletin, May 1990 discloses a comparator includes feedback that changes a logical level of the lock signal output to the host device when the value of the lock signal changes by some value greater than a hysteresis threshold value (see part 3 and figure 2). The disclosure further states that this scheme has the advantage of providing a stabilized

synchronization acquisition (part 3, lines 2-3). Because of this advantage it would have been obvious to one skilled in the art a the time of invention to incorporate the phase lock as disclosed by the IBM Technical Disclosure Bulletin, May 1990 into the invention of Lutz.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
    a. Meltzer (US Publication No.: 20030112915)
    b. Lee (US Publication No.: 20020094054)
    c. Eom (US Publication No.: 20020084859)
    d. Nishimura et al (US Patent No.: 6392641).

16. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

17. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed,

and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LINDA WONG whose telephone number is (571)272-6044. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Linda Wong
8/25/2009

/Shuwang Liu/
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